Google Scholar BETA

binary host information processing emulate "ei Search

Advanced Scholar Search
Scholar Preferences
Scholar Help

Scholar **All articles** Recent articles Results **1** - **10** of about **20** for **binary** **host** **information** **processing** **emu**

All Results
M Svancarek
H Suzuki
M Adan
M Van Flandern
J Pierce

System and method for the software emulation of a computer joystick - group of 2 »
MK Svancarek, ME Adan, MW Van Flandern, JG Pierce, ... - US Patent 5,793,356, 1998 - Google Patents
... SOFTWARE **EMULATION** OFA COMPUTER ... **host** computer may have bidirectional communication
with ... ticularly common with **entertainment software** such as com- ...
Cited by 28 - Related Articles - Web Search

A challenge for reusing multiplayer online games without modifying binaries - group of 2 »
Y Kaneda, H Takahashi, M Saito, H Aida, H Tokuda - Proceedings of 4th ACM SIGCOMM workshop on Network and ..., 2005 - portal.acm.org
... it is difficult to con- tinue **hosting** a gaming ... The port number and the **binary** name are described ... contexts by ap- pending each message to context **information**. ...
Cited by 2 - Related Articles - Web Search

Apparatus and method for bidirectional data communication in a game port - group of 2 »
MK Svancarek, ME Adan, MW Van Flandern, H Suzuki - US Patent 5,628,686, 1997 - Google Patents
... that a significant amount of computer **processing** time is ... Thus, the **host** computer must spend a signifi ... priately designated as **binary** devices since they typically ...
Cited by 15 - Related Articles - Web Search

Network Software Architectures for Real-Time Massively-Multiplayer Online Games - group of 2 »
RDP McFarlane - 2005 - digital.library.mcgill.ca
... **processing** for audio, data compression, electronic security, and ... **information** about the virtual world between participating nodes. The more ...
View as HTML - Web Search

[BOOK] Programming Lego Mindstorms with Java.:: the Ultimate Tool for Mindstorms Maniacs!
G Ferrari - 2002 - books.google.com
... editors for readers desiring additional reliable **information** on key ... the RCX ,ansion Kits rnative **Processing** Units 1 ... The Com mand-line 1eJOS **Emulator** Using the ...
Cited by 20 - Related Articles - Web Search - Library Search

Rising up from the MUD: inscribing gender in software design - group of 2 »
S Zdenek - Discourse & Society, 1999 - das.sagepub.com
... p. 12) implies an ongoing, highly regulated, **process** of identity ... coy', but 'usually divulges **information** if one ... ent across Mauldin's **binary** gender system ...
Cited by 4 - Related Articles - Web Search - BL Direct

COPYRIGHTED MATERIAL
G Accessibility, M Mail - language - media.wiley.com

... DNS, 1027 LDAP, 1026 NIS (Network **Information** System), 1026 ... folder types, netatalk
and, 941 **host** name, netatalk ... directory, 155 bin login, 372 **binary** RPMs, 183 ...
View as HTML - Web Search

System and method for dynamic data packet configuration - group of 2 »
MK Svancarek, ME Adan, MW Van Flandern, H Suzuki - US Patent 5,724,558, 1998 - Google Patents
... that a significant amount of computer **processing** time is ... of the timers.Thus, the **host** computer must ... priately designated as **binary** devices since they typically ...
Cited by 6 - Related Articles - Web Search

SEMINAR IN BUSINESS STRATEGY
B Strategies - tuta.hut.fi
... to compete for market share: Qualcomm's **Binary** Runtime Environment ...
INFORMATION AND
CONTENT (Non-Voice ... also possible to download an **emulator**-software called GoBoy ...

View as HTML - Web Search

Symbols & Numbers
G Accessibility, F ActiveX, M Mail - language - media.wiley.com
... bin login, 413 /bin directory, 165 **binary** RPMs, 205 ... file, 408 **hosts**.allow file, 408 **hosts**.deny file ... VPN, configuration, 673-676 contact **information**, domain name ...
View as HTML - Web Search

Google ▶
Result Page: 1 2 **Next**

Terms used **emulation entertainment software host computer** Found **379** of **196,064**

Sort results by relevance Save results to a Binder

Display results expanded form Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown Relevance scale

1 Analysis of hardware and software approaches to embedded in-circuit emulation of microprocessors

Hsin-Ming Chen, Chung-Fu Kao, Ing-Jer Huang

January 2002 **Australian Computer Science Communications , Proceedings of the seventh Asia-Pacific conference on Computer systems architecture CRPIT '02**, Volume 24 Issue 3

Publisher: Australian Computer Society, Inc., IEEE Computer Society Press

Full text available: pdf(665.32 KB) Additional Information: full citation, abstract, references, index terms

This paper investigates various approaches to embed the functionality of in-circuit emulation (ICE) into microprocessor cores in SoC (System-On-Chip) chips. Three styles of ICE's (hardware-oriented, software-oriented and hybrid) are defined and implemented. They are integrated with a synthesizable ARM7 microprocessor core and synthesized to gate level to quantitatively analyze and compare their performance, cost and debugging features.

2 Session 36: electrical and thermal issues in FPGAS: A fast HW/SW FPGA-based thermal emulation framework for multi-processor system-on-chip

David Atienza, Pablo G. Del Valle, Giacomo Paci, Francesco Poletti, Luca Benini, Giovanni De Micheli, Jose M. Mendias

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, index terms

With the growing complexity in consumer embedded products and the improvements in process technology, Multi-Processor System-On-Chip (MPSoC) architectures have become widespread. These new systems are complex to design as they must execute multiple complex applications (e.g. video processing, 3D games), while meeting additional design constraints (e.g. energy consumption or time-to-market). Moreover, the rise of temperature in the die for MPSoC components can seriously affect their final perform ...

Keywords: FPGA, MPSoC, emulation, thermal studies

3 Emulation of computer networks by microprogrammable microcomputers

David Cohen, Ming T. Liu

September 1974 **Conference record of the 7th annual workshop on Microprogramming MICRO 7**

Publisher: ACM Press
Full text available: pdf(430.27 KB) Additional Information: full citation, abstract, references, index terms

The advent of low cost, sophisticated, microprogrammable, LSI microprocessors has renewed interest in multiple-computer systems. This paper suggests a method of implementing microprogrammable microcomputer systems as a sophisticated tool (emulators) for decreasing the economic risk involved in development of large computer networks. Two levels of emulation are proposed for different network configurations. At the first level each microprocessor emulates one of the large computers in the rea ...

4 Techniques for Fast Transient Fault Grading Based on Autonomous Emulation
Celia Lopez-Ongil, Mario Garcia-Valderas, Marta Portela-Garcia, Luis Entrena-Arrontes
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '05**
Publisher: IEEE Computer Society
Full text available: pdf(97.22 KB) Additional Information: full citation, abstract, index terms

Very deep submicron and nanometer technologies have increased notably integrated circuit (IC) sensitiveness to radiation. Soft errors are currently appearing into ICs working at earth surface. Hardened circuits are currently required in many applications where Fault Tolerance (FT) was not a requirement in the very near past. The use of platform FPGAs for the emulation of single-event upset effects (SEU) is gaining attention in order to speed up the FT evaluation. In this work, a new emulation sy ...

5 An insight into PDP-11 emulation
J. C. Demco, T. A. Marsland
September 1976 **Proceedings of the 9th annual workshop on Microprogramming MICRO 9**
Publisher: ACM Press
Full text available: pdf(430.81 KB) Additional Information: full citation, abstract, references, citings, index terms

In order to evaluate the Nanodata QM-1 as a universal host computer, an emulator for a contemporary computer, the PDP-11, was designed and constructed. It was required that the emulator be functionally equivalent to the target, without making excessive sacrifices in emulation speed. Some properties of emulation hardware necessary to achieve these goals are identified. In addition, the paper describes a monitor designed to support different emulators concurrently on a single host machine.

6 Fast development of source-level debugging system using hardware emulation (short paper)
Sang-Joon Nam, Jun-Hee Lee, Byoung-Woon Kim, Yeon-Ho Im, Young-Su Kwon, Kyong-Gu Kang, Chong-Min Kyung
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation ASP-DAC '00**
Publisher: ACM Press
Full text available: pdf(204.60 KB) Additional Information: full citation, references

7 A user-microprogrammable, local host computer with low-level parallelism
Shinji Tomita, Kiyoshi Shibayama, Toshiaki Kitamura, Toshiyuki Nakata, Hiroshi Hagiwara
June 1983 **ACM SIGARCH Computer Architecture News , Proceedings of the 10th annual international symposium on Computer architecture ISCA '83**, Volume 11 Issue 3
Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(708.91 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the architecture of a dynamically microprogrammable computer with low-level parallelism, called QA-2, which is designed as a high-performance, local host computer for laboratory use. The architectural principle of the QA-2 is the marriage of high-speed, parallel processing capability offered by four powerful Arithmetic and Logic Units (ALUs) with architectural flexibility provided by large scale, dynamic user-microprogramming. By changing its writable control storage dy ...

Keywords: Firmware engineering, High-level language computer, Local host computer, Microprogrammable computer, Parallel processing

8 Solemn: Solaris Emulation Mode for Sparc Sulima

Bill Clarke

April 2004 **Proceedings of the 37th annual symposium on Simulation ANSS '04**

Publisher: IEEE Computer Society

Full text available: pdf(160.28 KB) Additional Information: full citation, abstract, index terms

In this paper we present Solemn, a new user-level simulationmode for Sparc Sulima, a SPARC V9 complete machinesimulator. Solemn extends Sparc Sulima allowing it tosimulate at user-level an unmodified Solaris executable: 32or 64-bit, and statically or dynamically linked. This yieldssome advantages over both complete machine simulatorsand traditional system call emulation. To do this, Solemnmanages the virtual address space and files that the simulatedprogram requires, and intercepts and emulates ...

9 On hardware enhanced 80386 software emulation, compiled emulation, a program distribution language, and pack computers

S. Lass

September 1989 **ACM SIGARCH Computer Architecture News**, Volume 17 Issue 5

Publisher: ACM Press

Full text available: pdf(218.87 KB) Additional Information: full citation, index terms

10 Debug Support, Calibration and Emulation for Multiple Processor and Powertrain Control SoCs

A. Mayer, H. Siebert, K. D. McDonald-Maier

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 3 DATE '05**

Publisher: IEEE Computer Society

Full text available: pdf(222.95 KB) Additional Information: full citation, abstract, index terms

The introduction of complex SoCs with multiple processor cores presents new development challenges, such that development support is now a decisive factor when choosing a System-on-Chip (SoC). The presented developments support strategy addresses the challenges using both architecture and technology approaches. The Multi-Core Debug Support (MCDS) architecture provides flexible triggering using cross triggers and a multiple core break and suspend switch. Temporal trace ordering is guaranteed down ...

11 A Diagnostic Emulator for HEAO software development

Peter H. Beer, Kenneth J. Hupf

July 1976 **ACM SIGSIM Simulation Digest , Proceedings of the 4th symposium on Simulation of computer systems ANSS '76**, Volume 7 Issue 4

Publisher: IEEE Press, ACM Press

Full text available: pdf(701.56 KB) Additional Information: full citation, abstract, references, index terms

Diagnostic Emulation is the application of microprogramming to the emulation of an operational computer to support software development and verification for that computer. A conventional technique, Interpretive Computer Simulation (ICS), has been used for many years in support of such software development and verification efforts. The ICS method is becoming less cost effective. For the development of attitude control software for NASA's High Energy Astronomical Observatory (HEAO) diagnostic ...

12 Performance evaluation and improvement of a dynamically microprogrammable computer with low-level parallelism

Shinji Tomita, Kiyoshi Shibayama, Toshiaki Kitamura, Hiroshi Hagiwara

November 1980 **ACM SIGMICRO Newsletter , Proceedings of the 13th annual workshop on Microprogramming MICRO 13**, Volume 11 Issue 3-4

Publisher: IEEE Press, ACM Press

Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, references, citings, index terms

A new microprogrammable computer with low-level parallelism was built and has been utilized as a research vehicle for solving different classes of research-oriented applications such as real-time processings on static/dynamic images, pictures and signals, and emulations of both existing and virtual machines including high (intermediate) level language machines. The design goal of a research-oriented computer, QA-1, was to achieve a high degree of processing power and system flexi ...

13 Virtual square (V^2) in computer science education

Renzo Davoli, Michael Goldweber

June 2005 **ACM SIGCSE Bulletin , Proceedings of the 10th annual SIGCSE conference on Innovation and technology in computer science education ITiCSE '05**, Volume 37 Issue 3

Publisher: ACM Press

Full text available: pdf(93.04 KB) Additional Information: full citation, abstract, references, index terms

It is common to name as *virtual* the imaginary space that can be created by software using computers and networks. This space is not only a set of processing and communications means and methods but it is also a space where humans can "meet," exchange ideas, leave messages etc. Students in computer science must learn how to design, implement, manage and debug the systems and networks that create this virtual space. Furthermore, CS students need an experimental environment --a playground-- ...

Keywords: administration, laboratory, networking, operating systems, security, teaching, virtual machine

14 Advances in accelerated simulation: Communication-efficient hardware acceleration for fast functional simulation

Young-Il Kim, Wooseung Yang, Young-Su Kwon, Chong-Min Kyung

June 2004 **Proceedings of the 41st annual conference on Design automation DAC '04**

Publisher: ACM Press

Full text available: pdf(199.10 KB) Additional Information: full citation, abstract, references, index terms

This paper presents new technology that accelerates system verification. Traditional methods for verifying functional designs are based on logic simulation, which becomes more time-consuming as design complexity increases. To accelerate functional simulation, hardware acceleration is used to offload calculation-intensive tasks from the software simulator. Hardware accelerated simulation dramatically reduces the simulation time. However, the communication overhead between the software simulator a ...

Keywords: communication overhead, functional verification, simulation acceleration

15 Applying parallel discrete event simulation to network emulation
Rob Simmonds, Russell Bradford, Brian Unger
May 2000 **Proceedings of the fourteenth workshop on Parallel and distributed simulation PADS '00**
Publisher: IEEE Computer Society
Full text available: pdf(767.64 KB) Additional Information: full citation, abstract, references, citings, index terms

The simulation of wide area computer networks is one area where the benefits of parallel simulation have been clearly demonstrated. Here we present a description of a system that uses a parallel discrete event simulator to act as a high speed network emulator. With this, real Internet Protocol (IP) traffic generated by application programs running on user workstations can interact with modelled traffic in the emulator, thus providing a controlled test environment for distributed app ...

Keywords: Internet protocol (IP), computer network emulation, conservative protocol, critical channel traversing, parallel discrete event simulation (PDES), real-time simulation

16 Evaluation of alternate data base machine designs
V. Vemuri, R. A. Liuzzi, J. P. Cavano, P. B. Berra
March 1980 **ACM SIGIR Forum , Proceedings of the fifth workshop on Computer architecture for non-numeric processing CAW '80**, Volume 15 Issue 2
Publisher: ACM Press
Full text available: pdf(788.11 KB) Additional Information: full citation, abstract, references, index terms

The purpose of this paper is to point out the need for performance evaluation measures and techniques suitable for the evaluation of specialized architectural features in nonnumeric applications. Toward this end, problems associated with the use of data base machines are examined at three levels of detail: the user level, the system level and the device level.

17 Microarchitecture-level power analysis and optimization techniques: Hybrid simulation for embedded software energy estimation
Anish Muttreja, Anand Raghunathan, Srivaths Ravi, Niraj K. Jha
June 2005 **Proceedings of the 42nd annual conference on Design automation DAC '05**
Publisher: ACM Press
Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, citings, index terms

Software energy estimation is a critical step in the design of energy-efficient embedded systems. Instruction-level simulation techniques, despite several advances, remain too slow for iterative use in system-level exploration. In this paper, we propose a methodology called *hybrid simulation*, which combines instruction set simulation with selective native execution (execution of some parts of the program directly on the simulation host computer), thereby overcoming the disadvantages of in ...

Keywords: embedded software, energy estimation, energy macromodels, hybrid simulation, pointers analysis

18 EASY—an operating system for the QM-1
Charles W. Flink

September 1977 **ACM SIGMICRO Newsletter , Proceedings of the 10th annual workshop on Microprogramming MICRO 10**, Volume 8 Issue 3
Publisher: IEEE Press, ACM Press

Full text available: pdf(733.19 KB) Additional Information: full citation, abstract, references, citings, index terms

The Emulation Aid SYstem is a virtual machine monitor for the Nanodata QM-1 microprogrammable computer. The system is designed to provide the user with an interactive interface for the development and subsequent use of emulations on the QM-1. EASY provides integrated support for: 1) interactive control of multiple, concurrently resident, virtual computers implemented via emulation, 2) input/output from emulations (virtual I/O) to the various real peripherals of the QM-1, and 3) diagnostic d ...

Keywords: Emulation, Intermediate language machines, Microprogramming, Nanodata QM-1, Software engineering, Virtual machine monitors, Virtual machines

19 Implementation aspects of a SPARC V9 complete machine simulator
Bill Clarke, Adam Czezowski, Peter Strazdins
January 2002 **Australian Computer Science Communications , Proceedings of the twenty-fifth Australasian conference on Computer science - Volume 4 ACSC '02**, Volume 24 Issue 1
Publisher: Australian Computer Society, Inc., IEEE Computer Society Press
Full text available: pdf(1.33 MB) Additional Information: full citation, abstract, references, index terms

In this paper we present work in progress in the development of a complete machine simulator for the UltraSPARC, an implementation of the SPARC V9 architecture. The complexity of the UltraSPARC ISA presents many challenges in developing a reliable and yet reasonably efficient implementation of such a simulator. Our implementation includes a heavily object-oriented design for the simulator modules and infrastructure, caching of repeated computations for performance, adding an OS (system call) emu ...

Keywords: SMP, SPARC V9 ISA, UltraSPARC, complete machine simulator, execution-driven simulation, object-oriented design

20 The Kiewit network: a large AppleTalk internetwork
R. E. Brown
August 1987 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM workshop on Frontiers in computer communications technology SIGCOMM '87**, Volume 17 Issue 5
Publisher: ACM Press
Full text available: pdf(1.42 MB) Additional Information: full citation, abstract, index terms

Dartmouth College's Kiewit Network connects nearly all of the computing resources on the campus: mainframes, minicomputers, personal computers, terminals, printers, and file servers. It is a large internetwork, based on the AppleTalk protocols. There are currently over 2900 AppleTalk outlets in 44 zones on campus. Over 90 minicomputers act as bridges between 177 AppleTalk twisted pair busses. This paper describes the extent and facilities of the current network; the extensions made to the A ...

Fast development of source-level debugging system using hardware emulation (short paper)

Full text Pdf (205 KB)

Source **with EDA Technofair Design Automation Conference Asia and South Pacific** archive
Proceedings of the 2000 conference on Asia South Pacific design automation table of contents
Yokohama, Japan
Pages: 401 - 404
Year of Publication: 2000
ISBN:0-7803-5974-7

Authors

Sang-Joon Nam	VLSI Systems Lab., Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology, Teajon, Korea
Jun-Hee Lee	VLSI Systems Lab., Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology, Teajon, Korea
Byoung-Woon Kim	VLSI Systems Lab., Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology, Teajon, Korea
Yeon-Ho Im	VLSI Systems Lab., Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology, Teajon, Korea
Young-Su Kwon	VLSI Systems Lab., Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology, Teajon, Korea
Kyong-Gu Kang	VLSI Systems Lab., Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology, Teajon, Korea
Chong-Min Kyung	MRI Divison, Medison Corporation, Teajon, Korea

Sponsors IEEE-CAS : Circuits & Systems
IPSJ : Information Processing Society of Japan
SIGDA: ACM Special Interest Group on Design Automation
IEICE : Inst of Electronics, Info & Communication Engineers

Publisher ACM Press New York, NY, USA

↑ REFERENCES

Note: OCR errors may be found in this Reference List extracted from the full text article. ACM has opted to expose the complete List rather than only correct and linked references.

1 R.A.Gott, "Debugging embedded software," Computer Design, pp.71-78, Feb. 1998.

2 IEEE, "IEEE Standard Test Port and Boundary-Scan Architecture," IEEE, 1990.

3 Jainendra Kumar , Noel R. Strader , Jeff Freeman , Michael Miller, Emulation verification of the

Motorola 68060, Proceedings of the 1995 International Conference on Computer Design: VLSI in Computers and Processors, p.150, October 02-04, 1995

4 G.J.Bunza, "The Impact of Hardware/Software Co-development on Design Process Methodology: Big Changes and Bigger Success," Proc. Design, Automation and Test in Europe, pp.37-41, Feb. 1998.

5 Gopi Ganapathy , Ram Narayan , Glenn Jorden , Denzil Fernandez , Ming Wang , Jim Nishimura, Hardware emulation for functional verification of K5, Proceedings of the 33rd annual conference on Design automation, p.315-318, June 03-07, 1996, Las Vegas, Nevada, United States

6 James Gateley , Miriam Blatt , Dennis Chen , Scott Cooke , Piyush Desai , Manjunath Doreswamy , Mark Elgood , Gary Feierbach , Tim Goldsbury , Dale Greenley, UltraSPARC-I, Proceedings of the 32nd ACM/IEEE conference on Design automation, p.13-18, June 12-16, 1995, San Francisco, California, United States

7 S.J.Nam et.al, "VLIW Geometry Processor for 3D Graphics Acceleration," International Symposium on Low-Power and High- Speed Chips (COOL Chips), pp.107-120, Apr. 1999.

8 Texas Instruments, "SN74ACT8990, Test-Bus Controllers IEE STD 1149.1 TAP masters with 16-bit Generic Host Interfaces," http://www.ti.com.

9 Quickturn Design Systems, Inc., "System Realizer User's Guide Version 5.0,"

↑ **Collaborative Colleagues:**

Yeon-Ho Im:	Chang-Young Han Kyong-Gu Kang Byoung-Woon Kim Lee-Sup Kim Young-Su Kwon Chong-Min Kyung Jun-Hee Lee Sang-Joon Nam			
Kyong-Gu Kang:	Yeon-Ho Im Byoung-Woon Kim Young-Su Kwon Chong-Min Kyung Jun-Hee Lee Sang-Joon Nam			
Byoung-Woon Kim:	Jang-Ho Cho Chan-Soo Hwang Seung-Ho Hwang Seung-Hoon Hwang Yeon-Ho Im Kyong-Gu Kang In-Hyung Kim Jae-Yeol Kim Jong-Sun Kim Jun-Sung Kim	Young-Su Kwon Chong-Min Kyung Dae-Hyun Lee Jong-Yeol Lee Jun-Hee Lee Kun-Moo Lee Yong-Hoon Lee Sang-Joon Nam Sang-Jun Nam In-Cheol Park	In-Cheol Park Kwang-11 Park Kyu-Ho Park Chang-Ho Ryu Sung-won Seo Jin-Hyuk Yang Hyun-Dhong Yoon	
Young-Su Kwon:	Jang-Ho Cho Chan-Soo Hwang Seung-Ho Hwang Seung-Hoon Hwang	Jun-Sung Kim Young-Il Kim Chong-Min Kyung Dae-Hyun Lee Jae-Gon Lee	Sang-Jun Nam Bong-Il Park In-Cheol Park In-Cheol Park Kwang-11 Park	Hyun-Dhong Yoon

	Yeon-Ho Im Kyong-Gu Kang Byoung-Woon Kim In-Hyung Kim Jae-Yeol Kim Jong-Sun Kim	Jong-Yeol Lee Jun-Hee Lee Kun-Moo Lee Yong-Hoon Lee Sang-Joon Nam	Kyu-Ho Park Chang-Ho Ryu Sung-won Seo Jin-Hyuk Yang Wooseung Yang	
Chong-Min Kyung:	Ki-Yong Ahn Seong-Ok Bae You-Sung Chang Jang-Ho Cho Hoon Choi Moo-Kyoung Chung Nak-Woong Eum Se-Kyoung Hong Chan-Soo Hwang Seung Ho Hwang Seung-Ho Hwang Seung-Hoon Hwang Yoon-Ho Hwang Yeon-Ho Im Kyong-Gu Kang	Ando Ki Byoung-Woon Kim In-Hyung Kim Jae-Yeol Kim Jong-Sun Kim Jun-Sung Kim Namseung Kim Suhwan Kim Taewhan Kim Young-Il Kim Peter V. Kraus Young-Su Kwon Dae-Hyun Lee Jae-Gon Lee Jong-Yeol Lee	Jun-Hee Lee Kun-Moo Lee Sang-Heon Lee Seungjong Lee Seungwang Lee Yong-Hoon Lee Dieter A. Mlynski Sang-Joon Nam Sang-Jun Nam Hun-Seung Oh Bong-Il Park Chang-Jae Park In-Cheol Park In-Cheol Park In-Cheolo Park	Kwang-11 Park Kyu-Ho Park Chang-Ho Ryu Sung-won Seo Heejun Shim Jin-Hyuk Yang Woo-Seung Yang Wooseung Yang Ju Hwan Yi Joon-Seo Yim Chi-Won Yoon Hyun-Dhong Yoon
Jun-Hee Lee:	Yeon-Ho Im Kyong-Gu Kang Byoung-Woon Kim Young-Su Kwon Chong-Min Kyung Sang-Joon Nam			
Sang-Joon Nam:	Chan-Soo Hwang Seung-Ho Hwang Yeon-Ho Im Kyong-Gu Kang Byoung-Woon Kim Young-Su Kwon Chong-Min Kyung Dae-Hyun Lee Jong-Yeol Lee Jun-Hee Lee	Yong-Hoon Lee In-Cheol Park Jin-Hyuk Yang		

↑ **Peer to Peer - Readers of this Article have also read:**

- Data structures for quadtree approximation and compression **Communications of the ACM** 28, 9
  Hanan Samet
- A hierarchical single-key-lock access control using the Chinese remainder theorem **Proceedings of the 1992 ACM/SIGAPP Symposium on Applied computing**
  Kim S. Lee , Huizhu Lu , D. D. Fisher
- The GemStone object database management system **Communications of the ACM** 34, 10
  Paul Butterworth , Allen Otis , Jacob Stein
- Putting innovation to work: adoption strategies for multimedia communication systems **Communications of the ACM** 34, 12
  Ellen Francik , Susan Ehrlich Rudman , Donna Cooper , Stephen Levine

- An intelligent component database for behavioral synthesis **Proceedings of the 27th ACM/IEEE conference on Design automation**
  Gwo-Dong Chen , Daniel D. Gajski

Terms used **emulation entertainment software master slave** Found **232** of **196,064**

Sort results by relevance
Display results expanded form
Save results to a Binder
Search Tips
Open results in a new window
Try an Advanced Search
Try this search in The ACM Guide

Results 41 - 60 of 200 Result page: previous 1 2 **3** 4 5 6 7 8 9 10 next
Best 200 shown Relevance scale

41 Running EveryWare on the computational grid

Rich Wolski, John Brevik, Chandra Krintz, Graziano Obertelli, Neil Spring, Alan Su
January 1999 **Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM) Supercomputing '99**
Publisher: ACM Press
Full text available: pdf(414.73 KB) Additional Information: full citation, references, citings, index terms

42 Specification and verification: Synthesis of system verilog assertions

Sayantan Das, Rizi Mohanty, Pallab Dasgupta, P. P. Chakrabarti
March 2006 **Proceedings of the conference on Design, automation and test in Europe: Designers' forum DATE '06**
Publisher: European Design and Automation Association
Full text available: pdf(178.14 KB) Additional Information: full citation, abstract, references

In recent years, Assertion-Based Verification is being widely accepted as a key technology in the pre-silicon validation of system-on-chip(SOC) designs. The System Verilog language integrates the specification of assertions with the hardware description. In this paper we show that there are several compelling reasons for synthesizing assertions in hardware, and present an approach for synthesizing System Verilog Assertions (SVA) in hardware. Our method investigates the structure of SVA propertie ...

43 Microprogramming: A step of a top-down design methodology

J. P. Schoellkopf
September 1974 **Conference record of the 7th annual workshop on Microprogramming MICRO 7**
Publisher: ACM Press
Full text available: pdf(324.77 KB) Additional Information: full citation, abstract, references, citings, index terms

Microprogramming is presented as a mean of implementing a given interpretation algorithm. Hardware architecture is approached in a top-down manner : it is considered as a mean of interpreting the previously defined microprogramming language. Microprogramming is presented as a peculiar level in a hierarchical organization of interpretation levels.

44 Explore multi-resolution views with PTZ and coordinated camera networks:

Surveillance camera scheduling: a virtual vision approach
Faisal Z. Qureshi, Demetri Terzopoulos
November 2005 **Proceedings of the third ACM international workshop on Video surveillance & sensor networks VSSN '05**
Publisher: ACM Press
Full text available: pdf(596.03 KB) Additional Information: full citation, abstract, references, index terms

We present a surveillance system, comprising wide field-of-view (FOV) passive cameras and pan/tilt/zoom (PTZ) active cameras, which automatically captures and labels high-resolution videos of pedestrians as they move through a designated area. A wide-FOV stationary camera can track multiple pedestrians, while any PTZ active camera can capture high-quality videos of a single pedestrian at a time. We propose a multi-camera control strategy that combines information gathered by the wide-FOV cameras ...

Keywords: camera control, camera scheduling, sensor coordination, surveillance systems, virtual vision

45 A variable instruction stream extension to the VLIW architecture
Andrew Wolfe, John P. Shen
April 1991 **ACM SIGARCH Computer Architecture News , ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the fourth international conference on Architectural support for programming languages and operating systems ASPLOS-IV**, Volume 19 , 25 , 26 Issue 2 , Special Issue , 4
Publisher: ACM Press
Full text available: pdf(1.25 MB) Additional Information: full citation, references, citings, index terms

46 Peer to peer: MOPAR: a mobile peer-to-peer overlay rrchitecture for interest management of massively multiplayer online games
Anthony (Peiqun) Yu, Son T. Vuong
June 2005 **Proceedings of the international workshop on Network and operating systems support for digital audio and video NOSSDAV '05**
Publisher: ACM Press
Full text available: pdf(243.91 KB) Additional Information: full citation, abstract, references, index terms

In this paper we propose a fully distributed peer-to-peer (P2P) infrastructure supporting Networked Virtual Environment (NVE) applications, such as massively multiplayer online games (MMOG). While many attempts have been made to tackle one of the most challenging issues in MMOGs - interest management, none of them are considered truly successful. Our architecture is a hybrid scheme focusing on NVEs' interest management. Our scheme takes the advantage of both structured overlay, i.e. Distributed ...

Keywords: interest management, massively multiplayer online games, networked games, networked virtual environment, peer-to-peer, scalable

47 The missing link: dynamic components for ML
Andreas Rossberg
September 2006 **ACM SIGPLAN Notices , Proceedings of the eleventh ACM SIGPLAN international conference on Functional programming ICFP '06**, Volume 41 Issue 9
Publisher: ACM Press
Full text available: pdf(263.53 KB) Additional Information: full citation, abstract, references, index terms

Despite its powerful module system, ML has not yet evolved for the modern world of

dynamic and open modular programming, to which more primitive languages have adapted better so far. We present the design and semantics of a simple yet expressive firstclass component system for ML. It provides dynamic linking in a type-safe and type-flexible manner, and allows selective execution in sandboxes. The system is defined solely by reduction to higherorder modules plus an extension with simple module-le ...

Keywords: components, distributed programming, dynamic linking, dynamic typing, modules, pickling, separate compilation, units

48 Architectures and performance analysis: Formal performance evaluation of AMBA-based system-on-chip designs

Gabor Madl, Sudeep Pasricha, Luis Angel D. Bathen, Nikil Dutt, Qiang Zhu

October 2006 **Proceedings of the 6th ACM & IEEE International conference on Embedded software EMSOFT '06**

Publisher: ACM Press

Full text available: pdf(770.05 KB) Additional Information: full citation, abstract, references, index terms

The ARM Advanced Microcontroller Bus Architecture (AMBA) is a widely used interconnection standard for SoC design. In order to support high-speed pipelined data transfers, AMBA supports a rich set of bus signals, making the analysis of AMBA-based embedded systems a challenging proposition. This paper makes two main contributions to the analysis and evaluation of AMBA-based SoC designs. The first contribution is to provide a method for the performance analysis and evaluation of AMBA-based SoC des ...

Keywords: model checking, performance evaluation, system-on-chip

49 A course in computer structures

Jonathan Allen

January 1976 **ACM SIGARCH Computer Architecture News , Proceedings of the 3rd annual symposium on Computer architecture ISCA '76**, Volume 4 Issue 4

Publisher: ACM Press

Full text available: pdf(479.24 KB) Additional Information: full citation, abstract, references, index terms

In this subject, we treat computer structure as an element of a group of interacting structures including the technology, algorithm, data, and programming language. In the belief that the best designs result when these structural factors "match" in a complementary manner, the influence of each of these domains is carefully studied at both the conceptual and descriptive levels. Thus a modular treatment of current technology is provided, as well as a thorough analysis of algorithm ...

50 Experimental polyprocessor system (EPOS)—operating system

Mamoru Maekawa, Isamu Yamazaki, Akio Tanaka, Akira Nakamura, Katsuyo Ishida

April 1979 **Proceedings of the 6th annual symposium on Computer architecture ISCA '79**

Publisher: ACM Press

Full text available: pdf(578.61 KB) Additional Information: full citation, abstract, references, citings, index terms

EPOS's operating system structure, firmware structure, functional distribution, and restructuring are described. EPOS processors are functionally specialized to user functions as well as operating system functions. The performance improvement by functional specialization is generally expected to be two-to-ten times. The objective of job scheduling is to maximize the total system performance by assigning each job to the best suited processor. For this purpose and for easy maintenance, jobs c ...

51 A decoupled scheduling approach for the GrADS program development environment
Holly Dail, Henri Casanova, Fran Berman
November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing Supercomputing '02**
Publisher: IEEE Computer Society Press
Full text available: pdf(153.55 KB) Additional Information: full citation, abstract, references, citings, index terms

Program development environments are instrumental in providing users with easy and efficient access to parallel computing platforms. While a number of such environments have been widely accepted and used for traditional HPC systems, there are currently no widely used environments for Grid programming. The goal of the Grid Application Development Software (GrADS) project is to develop a coordinated set of tools, libraries and run-time execution facilities for Grid program development.In this pape ...

52 Computer architecture at Johns Hopkins
Michael J. Flynn, Mrs. Carol Rogers
April 1972 **ACM SIGARCH Computer Architecture News**, Volume 1 Issue 2
Publisher: ACM Press
Full text available: pdf(681.82 KB) Additional Information: full citation

53 Hardware support for distributed objects in a hypercube
J. L. Kozarek
January 1988 **Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1**
Publisher: ACM Press
Full text available: pdf(813.20 KB) Additional Information: full citation, abstract, references, index terms

A survey of parallel programs written for an experimental hypercube indicates that while systolic dataflow programs map well to a hypercube, general purpose programs with random dataflow are seriously constrained by the cost of communication. This paper proposes the augmentation of the hypercube architecture with a special-purpose communications coprocessor that provides hardware support for distributed objects. We anticipate this will increase the efficiency of inter-process commun ...

54 Experiences with poker
David Notkin, Lawrence Snyder, David Socha, Mary L. Bailey, Bruce Forstall, Kevin Gates, Ray Greenlaw, Willian G. Griswold, Thomas J. Holman, Richard Korry, Gemini Lasswell, Robert Mitchell, Philip A. Nelson
January 1988 **ACM SIGPLAN Notices , Proceedings of the ACM/SIGPLAN conference on Parallel programming: experience with applications, languages and systems PPEALS '88**, Volume 23 Issue 9
Publisher: ACM Press
Full text available: pdf(944.46 KB) Additional Information: full citation, abstract, references, citings, index terms

Experience from over five years of building nonshared memory parallel programs using the Poker Parallel Programming Environment has positioned us to evaluate our approach to defining and developing parallel programs. This paper presents the more significant results of our evaluation of Poker. The evaluation is driving our next effort in parallel programming environment; many of the results should be sufficiently general to apply to other related efforts.

55 Session: Diffusive parallelism: a parallel programming model for large scale

distributed computation systems
Peter D. Stout, Brian N. Bershad
September 1992 **Proceedings of the 5th workshop on ACM SIGOPS European workshop: Models and paradigms for distributed systems structuring EW 5**
Publisher: ACM Press
Full text available: pdf(575.62 KB) Additional Information: full citation, abstract, references

The spread of networks and powerful workstations has created an attractive source of parallel computing power. We are exploring a new parallel programming model, called *diffusive parallelism*, designed specifically for use with large scale, distributed computation systems. The model provides a simple, yet powerful, abstraction to the programmer, while making it possible to build a secure, robust, distributed computation system in the presence of long delays, failure, and untrusted user pro ...

56 Poster abstracts: Parallel processing over mobile ad hoc networks of handheld machines
Michael J. Jipping, Gary Lewandowski
October 2001 **Proceedings of the 2nd ACM international symposium on Mobile ad hoc networking & computing MobiHoc '01**
Publisher: ACM Press
Full text available: pdf(156.72 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we describe the formatting guidelines for ACM SIG Proceedings.

57 Towards target-level testing and debugging tools for embedded software
Harry Koehnemann, Timothy Lindquist
October 1993 **Proceedings of the conference on TRI-Ada '93 TRI-Ada '93**
Publisher: ACM Press
Full text available: pdf(1.28 MB) Additional Information: full citation, references, index terms

58 The TurboDOS™ operating system
Keith H. Bierman
August 1984 **ACM SIGSMALL Newsletter**, Volume 10 Issue 3
Publisher: ACM Press
Full text available: pdf(596.11 KB) Additional Information: full citation, abstract

A commercially available multi-microcomputer system is described. Facilities and features are described from a user's standpoint. Several research problems are proposed.

59 Military applications: distributed modeling for military applications: Enabling 1,000,000-entity simulations on distributed Linux clusters
Gene Wagenbreth, Ke-Thia Yao, Dan M. Davis, Robert F. Lucas, Thomas D. Gottschalk
December 2005 **Proceedings of the 37th conference on Winter simulation WSC '05**
Publisher: Winter Simulation Conference
Full text available: pdf(576.61 KB) Additional Information: full citation, abstract, references

The Information Sciences Institute and Caltech are enabling USJFCOM and the Institute for Defense Analyses to conduct entity-level simulation experiments using hundreds of distributed computer nodes on Linux Clusters as a vehicle for simulating millions of JSAF entities. Included below is the experience with the design and implementation of the code that increased scalability, thereby enabling two orders of magnitude growth and the effective use of DoD high-end computers. A typical JSAF experime ...

60 Evaluation of user satisfaction and learnability for outdoor augmented reality gaming

Benjamin Avery, Wayne Piekarski, James Warren, Bruce H. Thomas

January 2006 **Proceedings of the 7th Australasian User interface conference - Volume 50 AUIC '06**

Publisher: Australian Computer Society, Inc.

Full text available: pdf(11.36 MB) Additional Information: full citation, abstract, references, index terms

We have developed an outdoor augmented reality game, Sky Invaders 3D, which is designed to be played by the game playing public. We conducted a user study to measure how much users enjoyed playing an outdoor AR game, and how intuitive it was. We compared 44 participants on one of two games, an outdoor AR game, or a desktop PC equivalent of the same game. We found the AR game was rated by the participants as significantly more enjoyable by the users and more intuitive to use.

Keywords: augmented reality, enjoyment, evaluation, gaming

Terms used **emulation entertainment software master slave** Found **232** of **196,064**

Sort results by relevance Save results to a Binder

Display results expanded form Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 41 - 60 of 200 Result page: previous 1 2 **3** 4 5 6 7 8 9 10 next

Best 200 shown Relevance scale

41 Running EveryWare on the computational grid

Rich Wolski, John Brevik, Chandra Krintz, Graziano Obertelli, Neil Spring, Alan Su

January 1999 **Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM) Supercomputing '99**

Publisher: ACM Press

Full text available: pdf(414.73 KB) Additional Information: full citation, references, citings, index terms

42 Specification and verification: Synthesis of system verilog assertions

Sayantan Das, Rizi Mohanty, Pallab Dasgupta, P. P. Chakrabarti

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Designers' forum DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(178.14 KB) Additional Information: full citation, abstract, references

In recent years, Assertion-Based Verification is being widely accepted as a key technology in the pre-silicon validation of system-on-chip(SOC) designs. The System Verilog language integrates the specification of assertions with the hardware description. In this paper we show that there are several compelling reasons for synthesizing assertions in hardware, and present an approach for synthesizing System Verilog Assertions (SVA) in hardware. Our method investigates the structure of SVA propertie ...

43 Microprogramming: A step of a top-down design methodology

J. P. Schoellkopf

September 1974 **Conference record of the 7th annual workshop on Microprogramming MICRO 7**

Publisher: ACM Press

Full text available: pdf(324.77 KB) Additional Information: full citation, abstract, references, citings, index terms

Microprogramming is presented as a mean of implementing a given interpretation algorithm. Hardware architecture is approached in a top-down manner : it is considered as a mean of interpreting the previously defined microprogramming language. Microprogramming is presented as a peculiar level in a hierarchical organization of interpretation levels.

44 Explore multi-resolution views with PTZ and coordinated camera networks:

Surveillance camera scheduling: a virtual vision approach
Faisal Z. Qureshi, Demetri Terzopoulos
November 2005 **Proceedings of the third ACM international workshop on Video surveillance & sensor networks VSSN '05**
Publisher: ACM Press
Full text available: pdf(596.03 KB) Additional Information: full citation, abstract, references, index terms

We present a surveillance system, comprising wide field-of-view (FOV) passive cameras and pan/tilt/zoom (PTZ) active cameras, which automatically captures and labels high-resolution videos of pedestrians as they move through a designated area. A wide-FOV stationary camera can track multiple pedestrians, while any PTZ active camera can capture high-quality videos of a single pedestrian at a time. We propose a multi-camera control strategy that combines information gathered by the wide-FOV cameras ...

Keywords: camera control, camera scheduling, sensor coordination, surveillance systems, virtual vision

45 A variable instruction stream extension to the VLIW architecture
Andrew Wolfe, John P. Shen
April 1991 **ACM SIGARCH Computer Architecture News , ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the fourth international conference on Architectural support for programming languages and operating systems ASPLOS-IV**, Volume 19 , 25 , 26 Issue 2 , Special Issue , 4
Publisher: ACM Press
Full text available: pdf(1.25 MB) Additional Information: full citation, references, citings, index terms

46 Peer to peer: MOPAR: a mobile peer-to-peer overlay rrchitecture for interest management of massively multiplayer online games
Anthony (Peiqun) Yu, Son T. Vuong
June 2005 **Proceedings of the international workshop on Network and operating systems support for digital audio and video NOSSDAV '05**
Publisher: ACM Press
Full text available: pdf(243.91 KB) Additional Information: full citation, abstract, references, index terms

In this paper we propose a fully distributed peer-to-peer (P2P) infrastructure supporting Networked Virtual Environment (NVE) applications, such as massively multiplayer online games (MMOG). While many attempts have been made to tackle one of the most challenging issues in MMOGs - interest management, none of them are considered truly successful. Our architecture is a hybrid scheme focusing on NVEs' interest management. Our scheme takes the advantage of both structured overlay, i.e. Distributed ...

Keywords: interest management, massively multiplayer online games, networked games, networked virtual environment, peer-to-peer, scalable

47 The missing link: dynamic components for ML
Andreas Rossberg
September 2006 **ACM SIGPLAN Notices , Proceedings of the eleventh ACM SIGPLAN international conference on Functional programming ICFP '06**, Volume 41 Issue 9
Publisher: ACM Press
Full text available: pdf(263.53 KB) Additional Information: full citation, abstract, references, index terms

Despite its powerful module system, ML has not yet evolved for the modern world of

dynamic and open modular programming, to which more primitive languages have adapted better so far. We present the design and semantics of a simple yet expressive firstclass component system for ML. It provides dynamic linking in a type-safe and type-flexible manner, and allows selective execution in sandboxes. The system is defined solely by reduction to higherorder modules plus an extension with simple module-le ...

Keywords: components, distributed programming, dynamic linking, dynamic typing, modules, pickling, separate compilation, units

48 Architectures and performance analysis: Formal performance evaluation of AMBA-based system-on-chip designs

Gabor Madl, Sudeep Pasricha, Luis Angel D. Bathen, Nikil Dutt, Qiang Zhu

October 2006 **Proceedings of the 6th ACM & IEEE International conference on Embedded software EMSOFT '06**

Publisher: ACM Press

Full text available: pdf(770.05 KB) Additional Information: full citation, abstract, references, index terms

The ARM Advanced Microcontroller Bus Architecture (AMBA) is a widely used interconnection standard for SoC design. In order to support high-speed pipelined data transfers, AMBA supports a rich set of bus signals, making the analysis of AMBA-based embedded systems a challenging proposition. This paper makes two main contributions to the analysis and evaluation of AMBA-based SoC designs. The first contribution is to provide a method for the performance analysis and evaluation of AMBA-based SoC des ...

Keywords: model checking, performance evaluation, system-on-chip

49 A course in computer structures

Jonathan Allen

January 1976 **ACM SIGARCH Computer Architecture News , Proceedings of the 3rd annual symposium on Computer architecture ISCA '76**, Volume 4 Issue 4

Publisher: ACM Press

Full text available: pdf(479.24 KB) Additional Information: full citation, abstract, references, index terms

In this subject, we treat computer structure as an element of a group of interacting structures including the technology, algorithm, data, and programming language. In the belief that the best designs result when these structural factors "match" in a complementary manner, the influence of each of these domains is carefully studied at both the conceptual and descriptive levels. Thus a modular treatment of current technology is provided, as well as a thorough analysis of algorithm ...

50 Experimental polyprocessor system (EPOS)—operating system

Mamoru Maekawa, Isamu Yamazaki, Akio Tanaka, Akira Nakamura, Katsuyo Ishida

April 1979 **Proceedings of the 6th annual symposium on Computer architecture ISCA '79**

Publisher: ACM Press

Full text available: pdf(578.61 KB) Additional Information: full citation, abstract, references, citings, index terms

EPOS's operating system structure, firmware structure, functional distribution, and restructuring are described. EPOS processors are functionally specialized to user functions as well as operating system functions. The performance improvement by functional specialization is generally expected to be two-to-ten times. The objective of job scheduling is to maximize the total system performance by assigning each job to the best suited processor. For this purpose and for easy maintenance, jobs c ...

51 A decoupled scheduling approach for the GrADS program development environment
Holly Dail, Henri Casanova, Fran Berman
November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing Supercomputing '02**
Publisher: IEEE Computer Society Press
Full text available: pdf(153.55 KB) Additional Information: full citation, abstract, references, citings, index terms

Program development environments are instrumental in providing users with easy and efficient access to parallel computing platforms. While a number of such environments have been widely accepted and used for traditional HPC systems, there are currently no widely used environments for Grid programming. The goal of the Grid Application Development Software (GrADS) project is to develop a coordinated set of tools, libraries and run-time execution facilities for Grid program development.In this pape ...

52 Computer architecture at Johns Hopkins
Michael J. Flynn, Mrs. Carol Rogers
April 1972 **ACM SIGARCH Computer Architecture News**, Volume 1 Issue 2
Publisher: ACM Press
Full text available: pdf(681.82 KB) Additional Information: full citation

53 Hardware support for distributed objects in a hypercube
J. L. Kozarek
January 1988 **Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1**
Publisher: ACM Press
Full text available: pdf(813.20 KB) Additional Information: full citation, abstract, references, index terms

A survey of parallel programs written for an experimental hypercube indicates that while systolic dataflow programs map well to a hypercube, general purpose programs with random dataflow are seriously constrained by the cost of communication. This paper proposes the augmentation of the hypercube architecture with a special-purpose communications coprocessor that provides hardware support for distributed objects. We anticipate this will increase the efficiency of inter-process commun ...

54 Experiences with poker
David Notkin, Lawrence Snyder, David Socha, Mary L. Bailey, Bruce Forstall, Kevin Gates, Ray Greenlaw, Willian G. Griswold, Thomas J. Holman, Richard Korry, Gemini Lasswell, Robert Mitchell, Philip A. Nelson
January 1988 **ACM SIGPLAN Notices , Proceedings of the ACM/SIGPLAN conference on Parallel programming: experience with applications, languages and systems PPEALS '88**, Volume 23 Issue 9
Publisher: ACM Press
Full text available: pdf(944.46 KB) Additional Information: full citation, abstract, references, citings, index terms

Experience from over five years of building nonshared memory parallel programs using the Poker Parallel Programming Environment has positioned us to evaluate our approach to defining and developing parallel programs. This paper presents the more significant results of our evaluation of Poker. The evaluation is driving our next effort in parallel programming environment; many of the results should be sufficiently general to apply to other related efforts.

55 Session: Diffusive parallelism: a parallel programming model for large scale

distributed computation systems
Peter D. Stout, Brian N. Bershad
September 1992 **Proceedings of the 5th workshop on ACM SIGOPS European workshop: Models and paradigms for distributed systems structuring EW 5**
Publisher: ACM Press
Full text available: pdf(575.62 KB) Additional Information: full citation, abstract, references

The spread of networks and powerful workstations has created an attractive source of parallel computing power. We are exploring a new parallel programming model, called *diffusive parallelism*, designed specifically for use with large scale, distributed computation systems. The model provides a simple, yet powerful, abstraction to the programmer, while making it possible to build a secure, robust, distributed computation system in the presence of long delays, failure, and untrusted user pro ...

56 Poster abstracts: Parallel processing over mobile ad hoc networks of handheld machines
Michael J. Jipping, Gary Lewandowski
October 2001 **Proceedings of the 2nd ACM international symposium on Mobile ad hoc networking & computing MobiHoc '01**
Publisher: ACM Press
Full text available: pdf(156.72 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we describe the formatting guidelines for ACM SIG Proceedings.

57 Towards target-level testing and debugging tools for embedded software
Harry Koehnemann, Timothy Lindquist
October 1993 **Proceedings of the conference on TRI-Ada '93 TRI-Ada '93**
Publisher: ACM Press
Full text available: pdf(1.28 MB) Additional Information: full citation, references, index terms

58 The TurboDOS[tm] operating system
Keith H. Bierman
August 1984 **ACM SIGSMALL Newsletter**, Volume 10 Issue 3
Publisher: ACM Press
Full text available: pdf(596.11 KB) Additional Information: full citation, abstract

A commercially available multi-microcomputer system is described. Facilities and features are described from a user's standpoint. Several research problems are proposed.

59 Military applications: distributed modeling for military applications: Enabling 1,000,000-entity simulations on distributed Linux clusters
Gene Wagenbreth, Ke-Thia Yao, Dan M. Davis, Robert F. Lucas, Thomas D. Gottschalk
December 2005 **Proceedings of the 37th conference on Winter simulation WSC '05**
Publisher: Winter Simulation Conference
Full text available: pdf(576.61 KB) Additional Information: full citation, abstract, references

The Information Sciences Institute and Caltech are enabling USJFCOM and the Institute for Defense Analyses to conduct entity-level simulation experiments using hundreds of distributed computer nodes on Linux Clusters as a vehicle for simulating millions of JSAF entities. Included below is the experience with the design and implementation of the code that increased scalability, thereby enabling two orders of magnitude growth and the effective use of DoD high-end computers. A typical JSAF experime ...

60 Evaluation of user satisfaction and learnability for outdoor augmented reality gaming

Benjamin Avery, Wayne Piekarski, James Warren, Bruce H. Thomas

January 2006 **Proceedings of the 7th Australasian User interface conference - Volume 50 AUIC '06**

Publisher: Australian Computer Society, Inc.

Full text available: pdf(11.36 MB) Additional Information: full citation, abstract, references, index terms

We have developed an outdoor augmented reality game, Sky Invaders 3D, which is designed to be played by the game playing public. We conducted a user study to measure how much users enjoyed playing an outdoor AR game, and how intuitive it was. We compared 44 participants on one of two games, an outdoor AR game, or a desktop PC equivalent of the same game. We found the AR game was rated by the participants as significantly more enjoyable by the users and more intuitive to use.

Keywords: augmented reality, enjoyment, evaluation, gaming